## REMARKS

This amendment is submitted in response to the Examiner's Action dated August 23, 2006, and pursuant to a telephonic conference between Applicants' representative and Examiner on October 20, 2006. In light of Examiner's statements with respect to the § 112, second paragraph, rejections, Applicants have amended the claims to more definitely claim all elements within Claims 1 and 11 and overcome the § 112 rejections. No new matter has been added, and the amendments place the claims in better condition for allowance and/or appeal. Applicants respectfully request entry of the amendments to the claims. The discussion/arguments provided below reference the claims in their amended form.

## CLAIMS REJECTIONS UNDER 35 U.S.C. § 112

In the present Office Action, Claims 1-20 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite. Upon further reading of the Action, only Claims 1 and 11 were noted by Examiner as containing indefinite matter. Applicants have amended these claims to more definitely recite all features contained therein. The claims now recite definite features, and thus the amendments overcome the § 112 rejection.

Specifically, with respect to Claim 1, the preposition "at" was replaced with "to", indicating that the input selection occurs prior to being received by the latches. That is, the input selection does not occur "at" the latches. As discussed during the telephonic conference, the "means," which performs the "selection" of the input at the single input latches is a selection circuitry coupled to the data input port of the latches. This selection circuit is the two-tiered NAND input circuit along with two clocks (CCLK, ACLK), as (a) illustrated by **FIGs. 2** and **3**, (b) described by Applicants' specification (e.g., para 0032-0034), and (c) expanded upon within Applicants' dependent claims (e.g., Claims 4-5). Given this clarification, which Examiner agreed made the claims more definite, Applicants respectfully request reconsideration and removal of the § 112 rejection in light of the amendments.

## CLAIMS REJECTIONS UNDER 35 U.S.C. § 102

In the present Office Action, Claims 1, 2, 3, 8 and 10 are rejected under 35 U.S.C. § 102(a) as being anticipated by *"Multiplexers and Demultiplexers"* (hereinafter *"Multiplexers"*). *Multiplexer* does not anticipate Applicants' claims because *Multiplexer* fails

to teach many of the features recited by Applicants' claims, particularly those features recited by independent Claim 1.

At the onset, Applicants note with interest that the amendment herein to Claim 1, which overcomes the § 112 rejections also clarifies the apparent mis-characterization (or mis-perception) of Examiner that the **single data input** latches are synonymous with a multiplexer. At page 5 of the Action, Examiner states that "for the purposes of examination the single input latches will be assumed to be a standard multiplexer." The premise behind which Examiner makes this assessment has been removed by the above mentioned amendments, which overcame the 112 rejection of Claim 1. Examiner appears to agree with this assessment during the telephonic conference.

*Multiplexer* simply provides a 2-to-1 MUX configuration with two select inputs (c1 and c0) utilized to trigger a connection of three MUXes, each having two data inputs. The MUXes provided by *Multiplexer* operate as standard MUXes with two data inputs and a select input. Applicants' invention clearly provides fuses, latches, and other circuit components that are coupled together. It is therefore clear that *Multiplexer* fails to teach the above listed and other features of Applicants' more complex circuit device, with a selection circuit that feeds latches having a single data input port.

As one skilled in the art recognizes, a multiplexer necessarily has **two data inputs** and a select input. Further, those skilled in the art recognize the inherent differences in functionality between a latch and a multiplexer, as both devices are utilized for different functions within the electronics/electrical arts.

Given that the premise of Examiner's entire rejections are based on consideration of each of Applicants' single input latches as a standard multiplexer, the clarification now provided eliminates *Multiplexer* as an appropriate 102 or 103 reference.

Applicants further reiterate the arguments presented in the previously-filed Amendment A. That is, with respect to *Multiplexers*, Examiner incorrectly attributes to that reference several

features recited within Applicants' claims which are neither taught nor suggested by *Multiplexers*. Among these features are the following:

(1) a first latch having a single data input port and a single clock input port and an output port;

(2) a second latch also having a single data input port and a single clock input port and an output port;

(3) means for ... selection of a scan chain input **to** said first latch and said second latch;

(4) means ... selection of a shift chain input **to** said first latch and said second latch; and

(5) wherein a selection of the scan chain input ... occurs exclusive of selection of the shift chain input..., and wherein said single data input latches provide functionality of latches that support multiple inputs.

The standard for a § 102 rejection requires that the references teach each element recited in the claims set forth within the invention. As clearly outlined above, both references fail to meet this standard and therefore neither reference anticipates Applicants' invention.

**CLAIM REJECTIONS UNDER 35 U.S.C. § 103**

In the present Office Action, Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Multiplexers* as applied to Claim 3 above, and further in view of *Esposito* (U.S. Patent No. 4,066,882). Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Multiplexers*. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over *Multiplexers* as applied to Claim 1 above, and further in view of Applicant's Admitted Prior Art *(AAPA)*. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over *Multiplexers* as applied to Claim 9 above, and further in view of *Maejima* (U.S. Patent No. 6,639,848). Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over *Multiplexers* and *AAPA*. Claims 15-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Multiplexers* or *AAPA* and as evidenced by *Esposito*.

Each of these claim rejections rely on the mischaracterization of the single input latches of Applicants' claimed invention as being synonymous with a multiplexer. As previously explained, this mischaracterization is incorrect, and *Multiplexer* is therefore not a valid reference to support any of the above rejections. Notably, each 103 rejection relies on *Multiplexer* as its

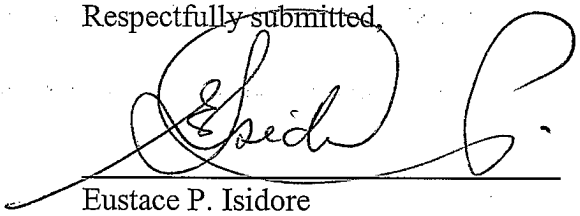
primary reference. Therefore, the present claims are not unpatentable over *Multiplexers* individually or in combination with any of the above listed references, and the above claims are allowable over the references and combinations thereof.

## CONCLUSION

Applicants have diligently responded to the Office Action by amending the claims to overcome the § 112 rejections. Applicants have also provided discussion/arguments which show that the primary reference is not an appropriate reference and that Applicants' claims are not anticipated by or obvious in light of that reference or the various combinations of references provided. Since the amendments and arguments overcome the §§ 112, 102 and 103 rejections, Applicants, respectfully request issuance of a Notice of Allowance for all claims now pending.

Applicants further respectfully request the Examiner contact the undersigned attorney of record at 512.343.6116 if such would further or expedite the prosecution of the present Application.

Respectfully submitted,



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